

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-5 (cancelled)

1 **Claim 6 (currently amended):** A plasma processing
2 method in which an electrode that is a conductor and has a
3 top surface that is greater in external size than a
4 substrate to be plasma-processed that has an insulating
5 layer on a front surface thereof is provided in a
6 processing room, the top surface of the electrode has a top
7 surface central area that is inside a boundary line that is
8 distant inward by a prescribed length from an outer
9 periphery of the substrate and in which the conductor is
10 exposed and a ring-shaped top surface peripheral area that
11 surrounds the top surface central area and in which the
12 conductor is covered with an insulating coating, and plasma
13 processing is performed in a state that the substrate is
14 held by the top surface of the electrode by electrostatic
15 absorption and the electrode is being cooled, **characterized**
16 in **comprising:**

17 **that the substrate is mounted mounting the substrate**
18 on the top surface of the electrode in such a manner that
19 a central portion and a peripheral portion of the

20 insulating layer of the substrate are in contact with the
21 top surface central area and the insulating coating in the
22 top surface peripheral area, respectively;

23 ~~that the substrate is electrostatically absorbed~~
24 electrostatically absorbing the substrate on the top
25 surface central area by mainly utilizing the central
26 portion of the insulating layer as a dielectric for
27 electrostatic absorption; and

28 ~~that the top surface central area of the electrode is~~
29 insulated insulating the top surface central area of the
30 electrode from plasma by bringing the outer peripheral
31 portion of the insulating layer into close contact with the
32 insulating coating.

1 **Claim 7 (original):** The plasma processing method
2 according to claim 6, wherein the substrate is a
3 semiconductor substrate on the front surface of which logic
4 circuits are formed, and that a back surface of the
5 semiconductor substrate is etched by the plasma processing.

1 **Claim 8 (original):** The plasma processing method
2 according to claim 7, wherein microcracks that have
3 developed on the back surface of the semiconductor
4 substrate in mechanical processing are etched away.